Universal Chiplet Interconnect Express (UCIe) Sideband: A Chisel Implementation, and Utilities for Chipyard integration

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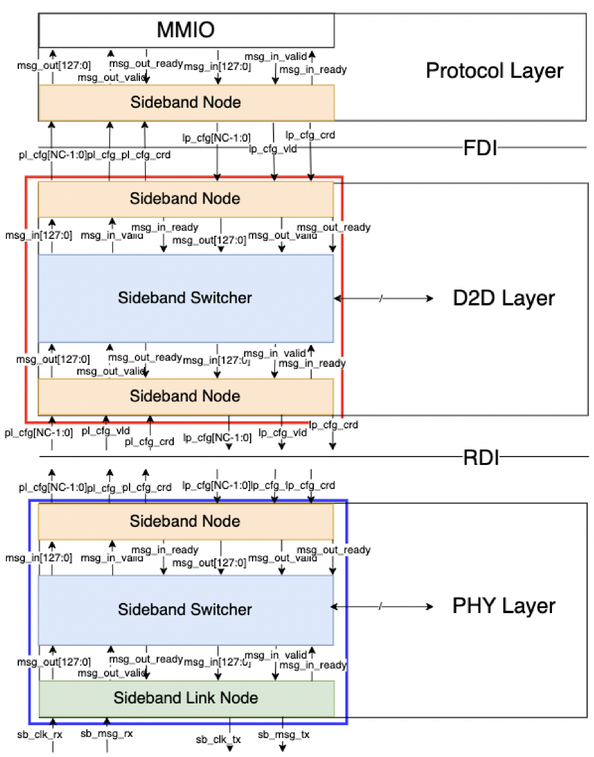
UCIe Universal Chiplet Interconnect Express

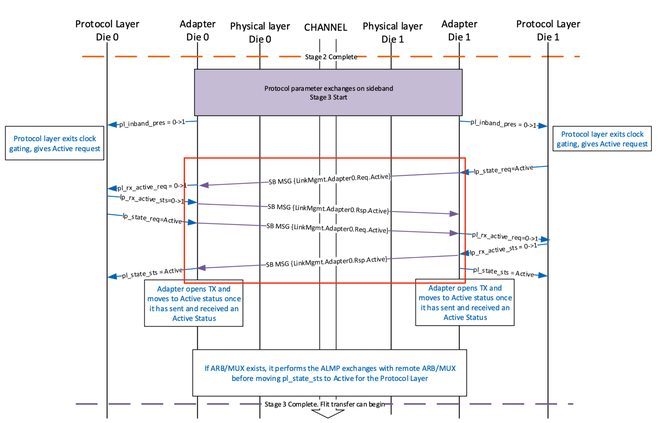
Overview

UCIe is an open, multi-protocol capable, on-package interconnect standard. **Sideband** provides a back-channel for Link **training**, access of **registers**, link **management** packets and **parameter** exchanges with remote Link partner.

Overall Architecture

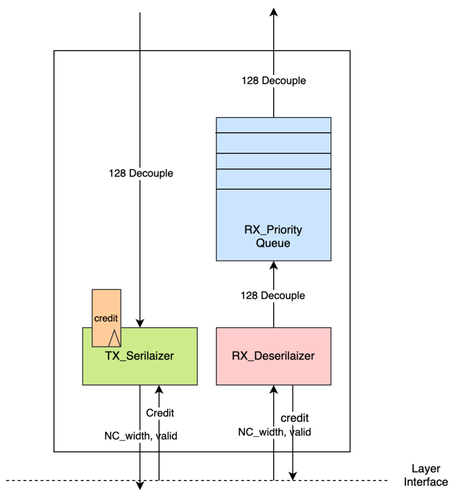


Example Usage

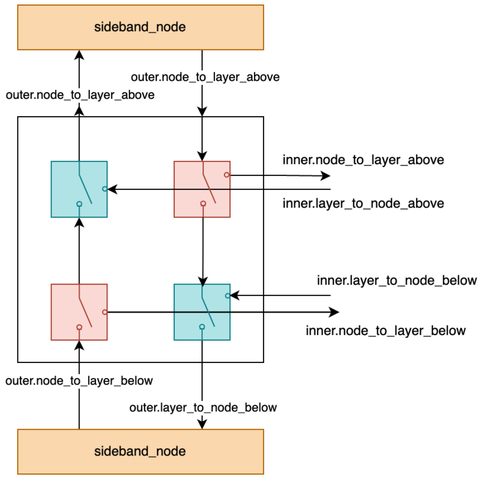


Implementations

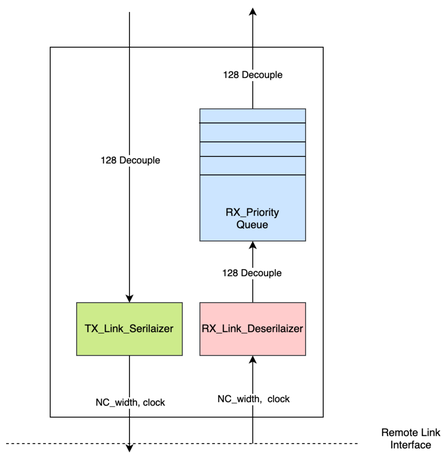
Sideband Node



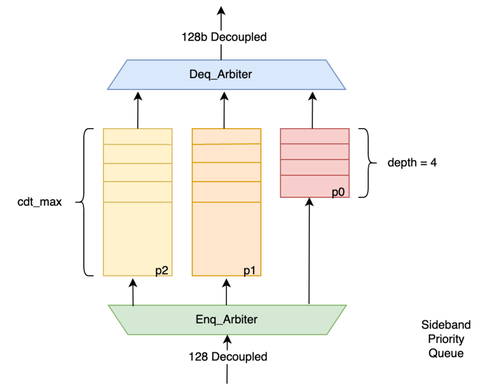
Sideband Swithcer



Sideband LinkNode



Priority Queue



Verification

Module	Test	Status
Unit Test	Every sub-module is unit-tested	PASS
Sideband Node	Check data from interface to layer and credit return	PASS
	Check data from layer to interface is correct	PASS
	Check not send req message when credit counter 0	PASS
	Check “completion” and “message” not get blocked	PASS
Sideband Link Node	Check data & clock output correct & stalling	PASS
	Check link node pair behavior is fully functional	PASS
Sideband Switcher	Pass matching packets to layer	PASS
	Pass through non-matching packets	PASS
	Racing sending from both node and layer	PASS
Sideband Channel	Stress Testing: Flow Control, Duplex transmit, Priority mix	PASS

Utility: Message Encoding

```
sb-msg-encoding.txt
nop_crd 39..32=0x00 21..14=0x00 4..0=0b10010
link_mgmt_rdi_req_active      39..32=0x01 21..14=0x01 4..0=0b10010
link_mgmt_rdi_req_l1          39..32=0x04 21..14=0x01 4..0=0b10010
link_mgmt_rdi_req_l2          39..32=0x08 21..14=0x01 4..0=0b10010
link_mgmt_rdi_req_link_reset  39..32=0x09 21..14=0x01 4..0=0b10010
link_mgmt_rdi_req_link_error  39..32=0x0A 21..14=0x01 4..0=0b10010
...
```

parse.py*

adapted from riscv-opcodes

```
def LINK_MGMT_RDI_REQ_ACTIVE = BitPat("b...")
```

sb-msg-encoding.scala

```
def LINK_MGMT_RDI_RSP_LINK_RESET   = BitPat("b????????????
```