CHENGYI ZHANG

+1(341) 766-9131 ◇ Berkeley, CA
iansseijelly@berkeley.edu ◇ Github Page ◇ Personal Site

EDUCATION

University of California, Berkeley, Bachelor of Arts, Computer Science — Expected 2023
GPA: **3.978**/4 (Dean's List)
Selected Coursework: **EECS151** Digital Design and Integrated Circuits, **CS152** Computer Architecture and Engineering, **ELENG105** Microelectronic Devices and Circuits, **EECS251B** Advanced Digital Circuits, **CS61C** Computer Architecture & Machine Structures, **ELENG140** Linear Integrated Circuits, **CS162** Operating System

EXPERIENCE

CPU Design Verification Intern — May 2023 - August 2023
Apple — *Cupertino, CA*

- Worked on verification infrastructure for CPU design verification.
- Worked on verification suites for memory-subsystem securities for future products.

RESEARCH PROJECTS

RoSÉ, HW-SW Cosimulation of Full-Stack Robotics SoC Evaluation Infrastructure — August 2022 - Now

- Paper presented at *ISCA 2023*, and received Distinguished Artifact Award.
- Integrated the experimental FireSim on-premises FPGA deployment.
- Designed experiments sweeping across different software and hardware architecture for the optimal design points.

CoSMo, Configurable Sensor Model for Robotics SoC Evaluation — January 2023 - Now

- Abstract, poster, and presentation presented at *MICRO 2023 Student Research Competition*, won third place.
- Designed and implemented parameterized sensor channel generator with various interface options.
- Designed and implemented hardware adapters and software drivers to support software-configurable, in-the-fly bandwidth throttling and latency injection.
- Designed experiments to evaluate system accuracy and investigate sensor rate limitation tradeoffs.

FireAxe, partitioned cycle-accurate FPGA accelerated RTL simulation — January 2023 - Now

- Established high-speed communication between Alveo U250 Accelerator Card FPGAs through the Interlaken 150G and Aurora 64B66B Vivado IP cores over QSFP ports and optical links.
- Extended the FireSim infrastructure to support communication over QSFP and successfully booted Linux.
- Evaluated the link round trip latency and simulation performance with a peak frequency of 1.6MHz.
- Extended the software simulation infrastructure to support direct-connect multi-FPGA debugging.

BaceQG, Boolean Algebra Circuit & Expression Question Generator. — September 2022 - December 2023

- Designed a rule-based question generator and devised a difficulty-balancing algorithm.
- Implemented the generator program and integrated it into an online assessment platform, Prairielearn.

Unique Variant, Prairielearn controlled-randomization framework — January 2023 - May 2023

- Led a team of 4, managed project progress, organized meetings, and provided necessary training.
- Designed and implemented the software architecture for achieving controlled randomization of question generation with minimal invasive changes to the front-end, and full backward-support capabilities.
- Implemented the back-end infrastructural changes.

COURSE PROJECTS

UCIe Sideband, high speed chiplets interconnect standard in Chipyard *EECS251B*

- Designed and Implemented the sideband channel and relevant modules.
- Designed and Implemented utilities for parsing sideband messages and factory methods for Chipyard Integration
- The Project received the 2023 Apple-sponsored class Design Award.

LCD Driver, high performance, low-power analog driver for LCD Display *EE140*

- Designed an analog folded telescopic differential amplifier for driving an RC-modeled LCD Display matrix.
- Reached a low power consumption of 0.542mW and a settling error of 0.105% within 180ns delay.
- The design has a full output voltage swing of 1.4V and a stable phase margin of 75 degrees. It has a PSRR of 51.5dB and a CMRR of 73dB, showing good noise rejection ratio.

RV32I CPU, single-core in-order RISC-V processor *EECS151*

- Designed and implemented a CPU with RISC-V instruction set architecture and a 3-stage pipeline using Verilog, ASAP-7nm technology, and simulated, verified, synthesized, and laid-out the design.
- Implemented a direct-mapped, write-back cache.

PUBLICATION

RoSÉ: A Hardware-Software Co-Simulation Infrastructure Enabling Pre-Silicon Full-Stack Robotics SoC Evaluation
Dima Nikiforov, Shengjun Chris Dong, **Chengyi Lux Zhang**, Seah Kim, Borivoje Nikolic, Yakun Sophia Shao
International Symposium on Computer Architecture (ISCA), June 2023
ISCA Distinguished Artifact Award
Artifacts Available, Artifacts Evaluated - Functional, Results Reproduced

CoSMo: A Realistic Configurable Sensor Channel Model for Pre-Silicon Full-Stack Robotics SoCs Evaluation
Chengyi Lux Zhang, Dima Nikiforov, Yakun Sophia Shao
International Symposium on Microarchitecture (MICRO) Student Research Competitions (SRC), October 2023
Student Research Competition 3rd place, undergraduate division

FireAxe: Partitioned FPGA-Accelerated Simulation of Large-Scale RTL Designs
Joonho Whangbo, Edwin Lim, **Chengyi Lux Zhang**, Kevin Anderson, Abraham Gonzalez, Raghav Gupta, Nivedha Krishnakumar, Sagar Karandikar, Borivoje Nikolic, Yakun Sophia Shao, Krste Asanovic
Under Submission

WORKSHOPS AND TUTORIALS

MICRO 2023 Toronto, Canada; October 2023
Dima Nikiforov, Shengjun Kris Dong, **Chengyi Lux Zhang**, Borivoje Nikolic, Yakun Sophia Shao. "Designing, Deploying, and Evaluating Full-Stack Robotics Systems With RoSÉ." Tutorial at MICRO 2023.

TEACHING EXPERIENCE

Academic Student Employee Jan 2022 - Present
UC Berkeley *Berkeley, CA*

- Computer Science Mentor, Junior Mentor, CS61C: Intro to Machine Structures, Spring 2022.
- Course Reader, EECS151: Digital Design, Fall 2022.
- Course Teaching Assistance, EECS151: Digital Design, Spring 2023: student rating *6.97/7*; Fall 2023.